

MEM-3 32K x 8 STATIC RAM

FEATURES:

- * 24 ADDRESS DECODING
- * FRONT PANEL OR FRONT PANEL LESS OPERATION
- * PHANTOM DISABLE
- * ADDRESSABLE IN 8K BOUNDARIES
- * BOARD DISABLED FOR UNLOADED RAM
- * EXPANDABLE IN 1K INCREMENTS
- * BIDIRECTIONAL BUSSING ON EITHER DI OR DO LINES
SO BOARD MAY BE USED AS THE UPPER OR LOWER 8
BITS IN THE S-100 16 BIT DATA BUSS. (2 boards
required for 16 bit buss.)
- * UP TO 4 WAIT STATES ON XRDY OR PRDY LINES.
- * GRID MATRIX PWR LINES, WELL BYPASSED WITH CAPACITORS
FOR LOW NOISE.

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CAUTIONS IN CONSTRUCTION

1. Install all sockets. This may be accomplished by using masking tape to hold down one row at a time then soldering alternate corners of each socket. After all are soldered in this way, go back and reflow each soldered corner while pressing the corner all the way down with a finger, so the socket is flush with the PC board. After all sockets are mounted this way go back and solder all pins. Use a minimal amount of solder to make good connection. Excess solder is wasteful and may cause shorts.

2. Install resistor packs. Pin 1 goes to the left of the board (board is oriented connector toward bottom with component side up).

3. Install all capacitors observing polarity on the tantalum/electrolytic capacitors.

4. Install regulators. Use the 4-40 mounting hardware. Use a star washer on top of the regulators. Mount screws so the head of screw is on the bottom of the board with the nut on top.

5. Install the wire wrap pins. These pins may be supplied in a strip. Cut to appropriate length and install.

6. Before installing board in computer, check for proper operation of regulators with a current limited power supply.

7. Install ICs and run a RAM check.

8. R1&R2. These resistors may be added to the MEM-3 to limit the power dissipation on the LM323. This will allow 500 to 750 ma to be bypassed around the LM323 which allows the use of higher power 2114s, and for higher voltages on the +8 volt. For information in calculation, the upper LM323 powers the upper 5 rows of ICs. The lower LM323 powers the rest. The support ICs consume about 400ma mostly concentrated in the 74LS240s and 74LS243s.

INSTALLATION

1. Addressing to 8K boundaries. Wire wrap from address pins to appropriate bank select pins.

(Refer to the chart below.)

Wire Wrap Group #4 (TS4)

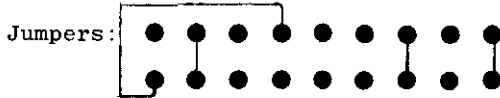
bank select

NC	BANK1	NC	BANK2	NC	BANK3	NC	BANK4
●	●	●	●	●	●	●	●
●	●	●	●	●	●	●	●
0000- 1FFF	2000- 3FFF	4000- 5FFF	6000- 7FFF	8000- 9FFF	A000- BFFF	C000- DFFF	E000- FFFF

address enable

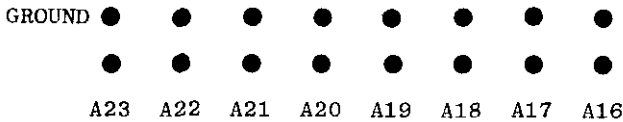
The board is only enabled for banks selected.

- Example: Bank 1 to 2000-3FFF
- Bank 2 to 0000-1FFF
- Bank 3 to A000-BFFF
- Bank 4 to E000-FFFF



2. Address to the upper 8 address lines. Wire wrap to ground each address. For comparison, a grounded connection corresponds to a low on the address line.

Wire Wrap Group 2 (TS2)



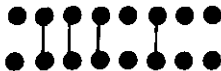
then on Wire Wrap group 3 (TS3) connect:



if this connection is not made, the upper 8 address lines are disregarded.

Example: Address board to 8BXXXX

Wire Wrap group 2 (TS2)



Wire Wrap group 3 (TS3)



3. Phantom. For phantom jumper

Wire Wrap Group #3 (TS3)



if this connection is not made, Phantom is disregarded.

4. Write Function. If MWRITE is used, then jumper Wire Wrap group #6 (TS6)



if \overline{PWR} is used, then jumper Wire Wrap group #6 (TS6)



5. Output Buffers. For normal operation using 8Bit DI&DO lines. Jumper Wire Wire Wrap Group #5 (TS5)



No connection on Wire Wrap Group 7

For bidirectional Data on DO lines, jumper Wire Wrap Group #5 (TS5)



and pull U14 and U15.

For bidirectional Data on DI lines, jumper Wire Wrap Group #7 (TS7)



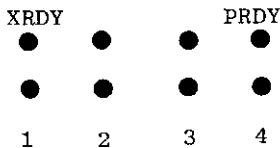
and pull U12 and U13.

6. Wait State.

NOTE: Wait states will only work properly when each bank of 8K is full. Wait states will also be applied if any RAM is

missing in that 8K. Therefore it is recommended that only RA that will operated with no wait states be used if this memor is used in less than 8K bound aries.

Wire Wrap Group #1 (TS1)

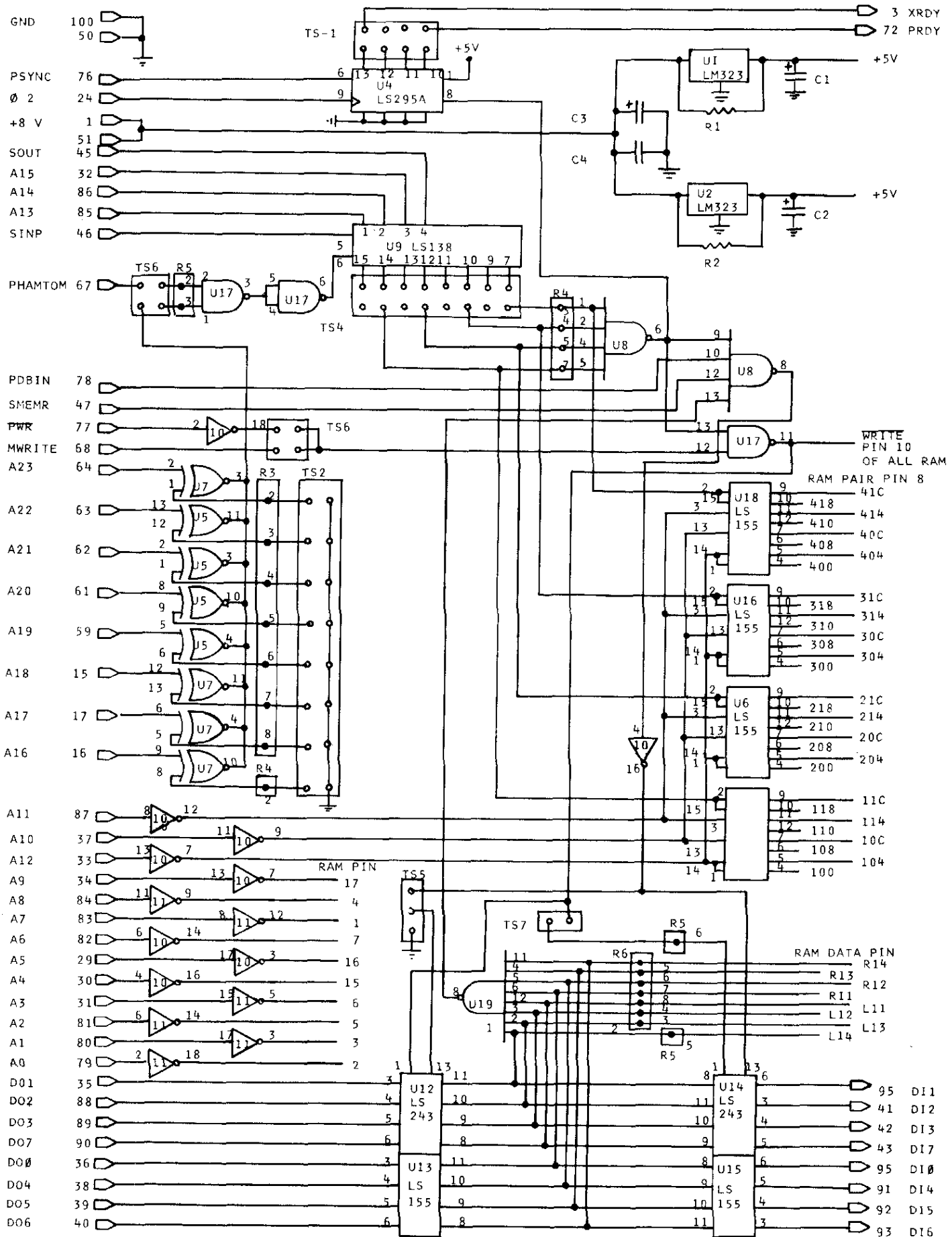


AT 2MHZ
 1 wait = 500nsec
 2 wait = 1000nsec
 3 wait = 1500nsec
 4 wait = 2000nsec
 no wait no connection

no Wait States are applied if no connection is made.

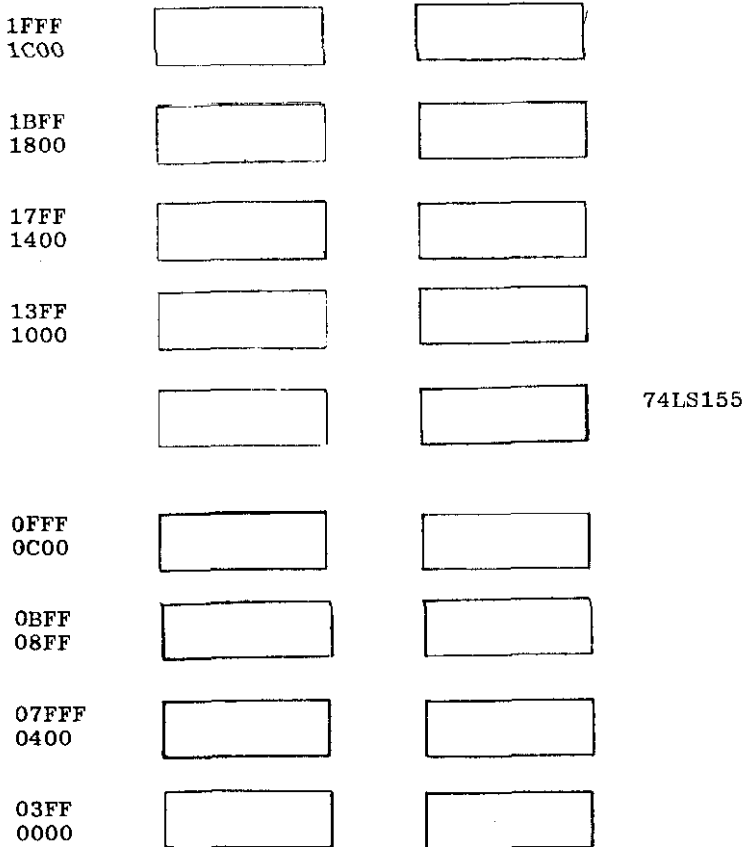
Example: 1 usec at PRDY





7. Less than 8K. By removing RAM the output buffers are disabled and allows PROMs on an appropriately designed PROM board to be used. As many holes as desired may be put into this board without affecting its operation. Each bank is

oriented with the lower address at the bottom and the upper address at the top. (NOTE: The left and right most banks are broken by 74LS155. These may be disregarded in the pattern of RAM location. This function may be defeated by removing U19.)



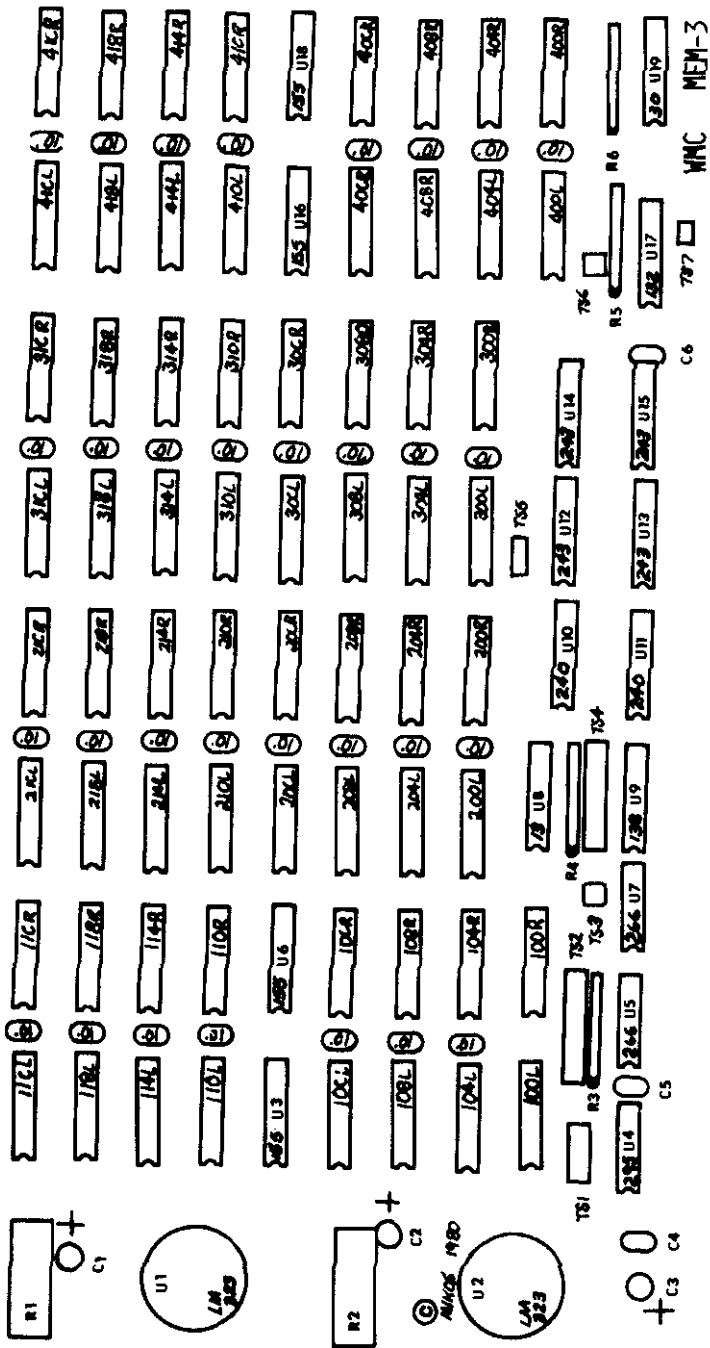


Figure 2. Parts Placement

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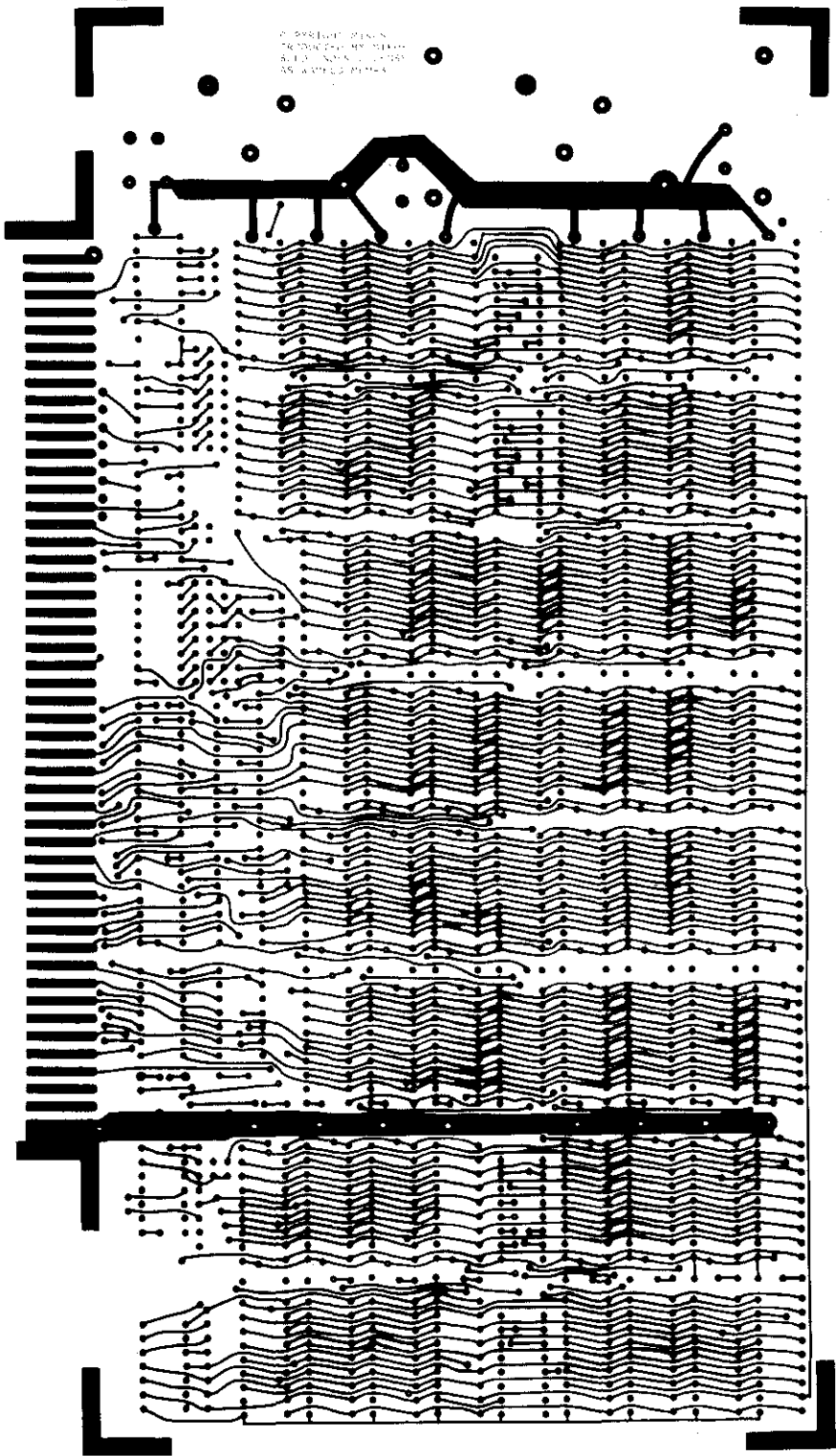


Figure 3. Component Side

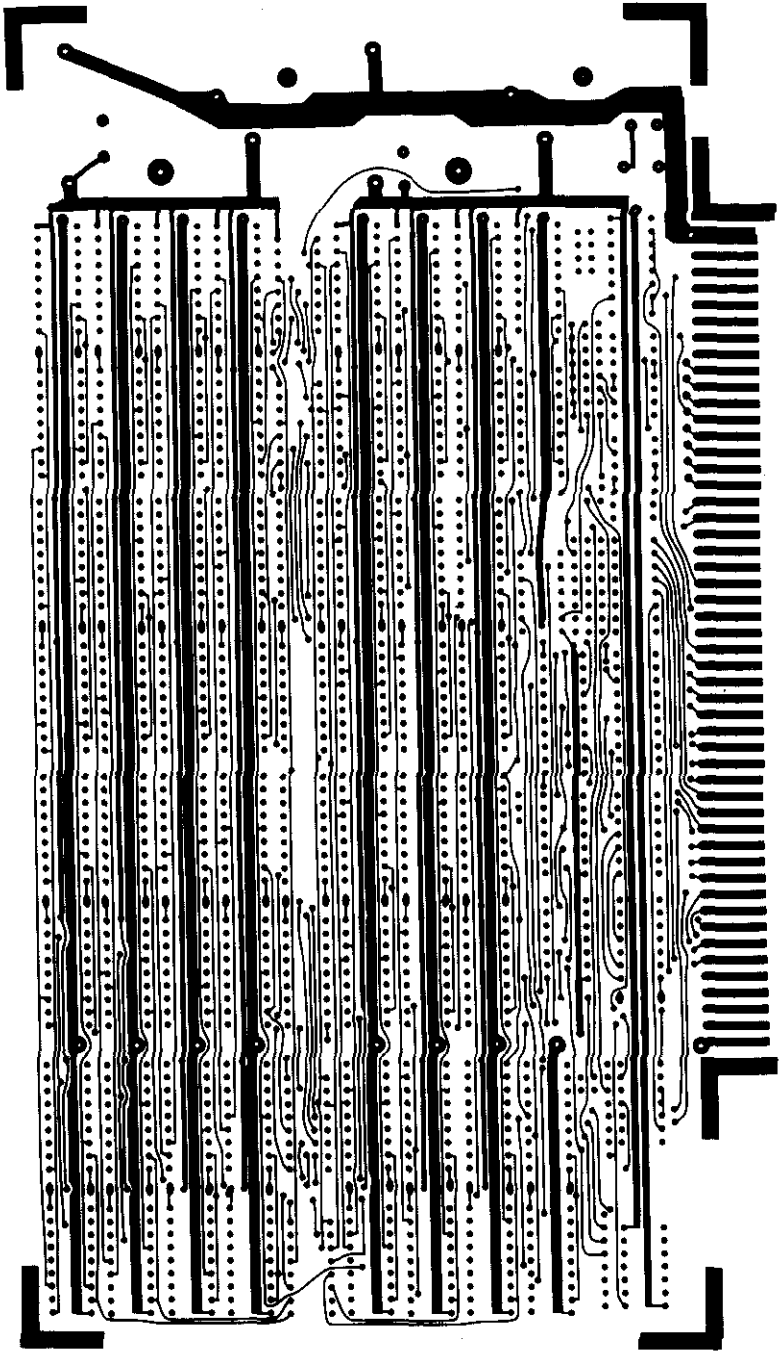


Figure 4. Solder Side
10.

8. The MIKOS ENGINEERING product you have purchased is guaranteed for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by MIKOS ENGINEERING, pre-paid freight, the board will be cheerfully replaced and the shipping charges incurred by you will be repaid. The guaranty is limited to replacement of the board with an equivalent board, even though the board may be defective through negligence in manufacturing or through other fault.

9. For future reference, a print of the front and back traces of the MEM-3 is shown.

10. We sincerely hope that the MEM-3 will give you long and satisfactory service. If you have any problems with the MEM-3, or if you just want to comment on the board, please write to me personally.

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